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To synthesize your design to a Spartan3E, you will need to download the Free ISE WebPACK from Xilinx Inc. The Xilinx synthesis tools are called from within the Aldec Active-HDL integrated GUI. We will use the Adept 2 (from Diligent) utility to download your synthesized design to the Xilinx FPGA.

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Digital Design Using Diligent FPGA Boards Resource Center. The reality is that today digital systems are designed by writing software in the form of hardware description languages HDLs. When you compile digllent block diagrams, the corresponding Verilog code is automatically generated.

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The book begins with an introduction to digital design and FPGA architecture in chapters 1-2. It then delves into getting started with Vivado Design Suite, and using the popular hardware description languages (VHDL and Verilog). Chapters 7-10 include an introduction to typical digital circuits and

elements in digital design circuits.

Digital System Design With FPGA: Textbook ... - Diligent Blog

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Digital System Design with FPGA: Implementation Using Verilog and VHDL begins with basic digital design methods and continues, step-by-step, to advanced topics, providing a solid foundation that allows you to fully grasp the core concepts. Real-life examples, start-to-finish projects, and ready-to-run Verilog and VHDL code is provided throughout.

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In over 75 examples we show you how to design digital circuits using VHDL and simulate and synthesize them using Xilinx's free development environment, Vivado HL WebPACK. You can synthesize the designs to a Xilinx Spartan3E FPGA on either the BASYS™ system board that can be purchased from Diligent, Inc (www.digilentinc.com) or any of the Nexys boards.

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