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The ARM University Program, ARM Architecture Fundamentals

ARM Assembly Language Part-I *EEVblog #1132 - The 3 Cent Microcontroller!* ARM Cortex-M3 Tutorial 11: Bit Banding

Cortex-M4 FPU and DSP instruction usage in the STM32F4 family

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CES2009 ARM Cortex-A8 processor-based Netbook from Freescale and Pegatron **Архитектура ARM Cortex** *Arm: New Endpoint AI Technologies: the Arm Cortex-M55 processor and Ethos-U55 microNPU*

Cortex R4 Technical Reference Manual

See the CoreSight ETM-R4 Technical Reference Manual. 1.2.3 Advanced Microcontroller Bus Architecture This Cortex-R4 processor complies with the AMBA 3 protocol. See AMBA AXI Protocol

Specification and AMBA 3 APB Protocol Specification. 1.2.4 Debug architecture The Cortex-R4 processor implements the ARMv7 Debug architecture that includes support for CoreSight.

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Cortex-R4 and Cortex-R4F Technical Reference Manual: Revision: r1p4: Home > System Control > Register descriptions > Cache operations: 4.3.21. Cache operations. The purpose of c7 is to manage the associated caches. The maintenance operations are formed into two management groups: Set and Way:

Cortex-R4 and Cortex-R4F Technical Reference Manual: 4.3 ...

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Cortex-R4 - Arm Developer

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Cortex-R4 - Arm

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ARM Cortex-R - Wikipedia

This book is for Cortex-R5 processors. Note • The Cortex-R5F processor is a Cortex-R5 processor that includes the optional Floating Point Unit (FPU) extension. • In this book, references to the Cortex-R5 processor also apply to the Cortex-R5F processor, unless the context makes it clear that this is not the case. Product revision status

Cortex-R5 Technical Reference Manual

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